Amendments to the Drawings

The attached sheet of drawings includes the requested changes to FIGs. 1A, 1B, and 1C.

Remarks/Arguments

This Amendment is in response to the Final Office Action mailed 29.11.2004 (29 November 2004). Specifically, the Examiner rejected claims 21, 22, 24-28, 30-33, 35-38, and 40 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089). Additionally, the Examiner rejected claims 23, 28, 33, and 38 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547).

1. Summary of Current Claims

Claims 21-40 have been canceled. In addition, Claims 1-20 were canceled in the prior amendment. Claims 41-46 are newly added claims.

2. Applicant Admitted Prior Art

In the Office Action , the Examiner classified parts of the disclosure as Applicant Admitted Prior Art (AAPA), and used the AAPA as part of the rejection of the claims under 35 USC 103(a). Specifically, the Examiner made the determination that the specification, p. 4, l. 15-23 and p. 6, l. 19 - p. 7, l. 2 teaches an internal bus in an SOC having a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any single initiator and any signal target. Additionally, the Examiner made the determination that the specification, p. 5, l. 9 -12 and p. 6, l. 19 - p. 7, l. 2 teaches that the coupling of the first internal bus further comprises adding an arbitrary

number of pipeline stages between any signal initiator and any signal target when floorplanning a single integrated circuit.

The Examiner took one paragraph that describes pipelining in general and parts of two other paragraphs that describe the problem solved by this invention, combined them together, and made the determination that the Applicant admitted it as prior art. In effect, the Examiner is taking the position that the part of the specification that Applicant uses to describe the problem solved by the invention is prior art against the Applicant's invention.

The Examiner uses the following paragraph as part of the AAPA:

> [08] The common solution to the problem of extended signal propagation times caused by the physical interconnect is pipelining – reducing the distance that must be traversed within a single clock cycle by inserting a flip-flop (also referred to herein as a register) in the path to capture and re-launch the signal. In other words, the pipelined signal travels from the source gate to the ultimate recipient gate within two clock cycles—from the signal source to the flip-flop during the first cycle, and from the flip-flop to the recipient during the second clock cycle. More flip-flops can be added in the signal path as required to further decrease the distance the signal must propagate in a single clock cycle, thus enabling shorter and shorter clock cycles (and thus higher and higher speed operation.)
>
> Specification, p. 4, l. 15-23.

The above paragraph discusses in general using registers as part of pipelining.

The Examiner additionally uses the following 2 segments that are taken out of context as other parts of the AAPA. The Applicant is including the full paragraphs of the segments to show how out of context the segments actually are:

> [09] However, those skilled in the art understand that this pipelining does have its own drawbacks. First, there is a point of diminishing returns. Adding pipeline stages to enable higher-speed operation can decrease the overall performance of the chip, even though it may be running faster, by introducing more opportunities for the chip to stall while awaiting the arrival of a deeply-pipelined signal at a critical gate. Moreover, since the delay between a signal's source gate and recipient gate is not known until after floorplanning, layout, and/or delay extraction of the chip, designers may not become aware that they have a signal distance problem, hence an operating frequency limitation, until relatively late in the design process. Adding unplanned-for pipeline

> stages this late in the design process can cause logic timing and synchronization problems, which then require some degree of redesign. The usual result is that the chip design and layout processes are iterative, often requiring several passes before an optimum design/layout balance is reached.
>
> Underlined is p. 5, l. 9-12.
>
> [12] In designing an SOC, chip designers strive to balance chip functionality, operating frequency and power, and chip size. Some features can only be achieved at the expense of others. Obviously, the on-chip interconnects must be designed to work even when other chip characteristics, such as size and maximum operating frequency, are unknown. For the reasons described above, SOC designers typically want to avoid having to add unplanned-for pipeline stages at the floorplanning stage, but because SOC designers never know the ultimate size of their designs until floorplanning is complete, stages often have to be added at the last minute. This initiates the undesirable iterative design/layout procedure described above, adding to the cost of the chip and delaying the time-to-market. A design architecture that is impervious to the last-minute addition of pipeline stages would be highly desirable, because pipeline stages could be added at floorplanning to address logic timing issues and operating frequency limitations without initiating another round of design and layout. Such an architecture technology would allow the number of pipeline stages to be defined after the chip size is known, rather than before.
>
> Underlined is p. 6, l. 19 – p. 7, l. 2.

The above 2 paragraphs, even though they are cited by the Examiner, describes the problems solved by the present invention.

The Applicant therefore respectfully requests that the Examiner withdraw the determination that the above represents Applicant Admitted Prior Art.

3. Claim Rejections under 35 USC 103(a)

The Examiner rejected claims 21, 22, 24-28, 30-33, 35-38, and 40 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089). In response to the Office Action, Applicant is amending and reordering the claims to further clarify the claimed invention. Applicant believes that these amendments place the pending claims in immediate condition for allowance or appeal.

The Examiner asserts that Hoffman teaches an SOC apparatus that includes one or more processor cores, one or more peripherals, and a first internal bus that couples

the processor cores and peripherals and carries signals from signal initiators to signal targets. And again, the Examiner concedes that Hoffman does not teach the use of an architecture with latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target that can be added during the floorplanning stage of the semiconductor device without requiring a subsequent design or floorplanning iteration.

The Examiner asserts that LaBerge provides one skilled in the art of designing SOCs with the knowledge to selectively connect some type of programmable circuits to the connection circuitry without requiring a fundamental redesign of the chip. The Examiner fails to consider that LaBerge and the present invention solve two completely separate problems. The ASIC (Application Specific Integrated Circuit) of LaBerge is a general type of semiconductor device that can be "programmed" by a user for a variety of tasks. The programming basically involves selectively "blowing" bits or pathways in the ASIC so that it then performs its function. Thus, the invention of LaBerge relates to a method for constructing a standard cell ASIC and a structure for a standard cell ASCI that speeds metal mask changes and permits logic changes by programming configuration bits.

The present invention is far more complicated than the ASIC of LaBerge. An SOC (System on a Chip) is taking one or more microprocessor "soft" cores and then connecting them to one or more different types of peripherals using one or more internal (to the SOC) busses. The single semiconductor device is created by the process of connecting all of the cores and peripherials together. This process is akin to taking what used to be a number of separate semiconductor devices on a computer board and

stuffing them altogether into a single chip. As described above, the present invention solves a problem in the connection of the peripherals to the cores via the internal busses by allowing a designer to add in as needed pipeline stages during the floorplanning stage to address/correct timing issues without the need to initiate another round of design and layout.

And, as discussed above, the Examiner erred in making a determination that the Applicant created AAPA within the discussion of the specification.

Therefore, the Examiner has failed to establish a prima facie case of obviousness for using non-existent AAPA, Hoffman, and LaBerge, or their combination as 103(a) references. To establish a prima facie case of obviousness, an Examiner must met 3 basic criteria:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> MPEP 2143.

When an Examiner is applying 35 USC 103, the Examiner must consider and follow the following standards:

> When applying 35 USC 103, the following tenets of patent law must be adhered to:
> (A) The claimed invention must be considered as a whole;
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and
> (D) Reasonable expectation of success is the standard with which obviousness is determined.
>
> MPEP 2141

The Examiner has not considered the claimed invention as a whole. Additionally, the Examiner has failed to consider all elements and limitations of Applicant's claims. This results in the failure of non-existent AAPA, Hoffman, and LaBerge not teaching or suggesting all of the claim elements and limitations of the claimed invention either individually or in combination. Principally, none of the cited references, either alone or in combination teach an SOC design architecture with a latency tolerant signal protocol that carries signals from signal initiators to signal targets in an SOC where the latency tolerant signal protocol provides for an arbitrary number of pipeline stages between any signal initiator and any signal target where the arbitrary number of pipeline stage(s) are added during the floorplanning of the semiconductor device without requiring a subsequent design or floorplanning iteration.

Since the present claims include elements and limitations that are not shown, taught, or implied by the prior art, Applicant therefore respectfully requests that the Examiner withdraw the rejections to claims 21, 22, 24-28, 30-33, 35-38, and 40 under 35 USC 103(a) as being unpatentable over Hoffman et al. (US Pat. No. 6,513,089), Applicant Admitted Prior Art (AAPA), and LaBerge (US Patent No. 6,513,089).

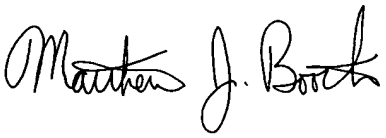
The Examiner additionally rejected claims 23, 28, 33, and 38 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547). As previously discussed, the failure of non-existent AAPA, Hoffman, and LaBerge not teaching or suggesting all of the claim elements and limitations of the claimed invention either individually or in combination means that these are not proper 103(a) references, and thus when combined with

Sheafor, Quereshi, and Pawlowski still do not make a prima facie case for obviousness. Applicant therefore respectfully requests that the Examiner withdraw the rejections to claims 23, 28, 33, and 38 as being unpatentable under 35 USC 103(a) over Hoffman, AAPA, and LaBerge, in view of Sheafor et al. (US Patent No. 6,493,407), Quereshi et al. (US Patent No. 6,173,349), and Pawlowski et al. (US Patent No. 5,469,547).

4. Summary

In view of the above, Applicant believes that each of the presently pending claims is in immediate condition for allowance or appeal. Accordingly, Applicant respectfully requests that the Examiner withdraw the outstanding objections and rejections of the claims and issue a timely Notice of Allowance in this case.

Respectfully submitted,



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Replacement Drawing Sheet